

# *Logic Emulator with Routing Chip providing Virtual Full-Crossbar Interconnect*

## **Abstract of Disclosure**

A hardware-based logic emulator uses routing chips to implement a virtual full-crossbar interconnect. Logic gates and some internal interconnection of the emulated design are programmed into field-programmable gate array (FPGA) logic chips. External interconnection of the logic chips is provided by routing chips. When the routing chips are also FPGA chips with a same number of I/O pins, the number of routing chips can be 1.5 times the number of logic chips. For  $L$  logic chips, the first  $L$  routing chips are column routing chips. The column routing chips connect to the same pin or pins of all the logic chips and make connections within a single column of a routing table. The other  $L/2$  routing chips are diagonal routing chips that connect to different pins on different logic chips. The diagonal routing chips make connections among logic chips along diagonals in the routing table.